



LA-6741P
DA60000JE10

Compal Confidential

Brazos PCM10 LA6741 Schematics Document

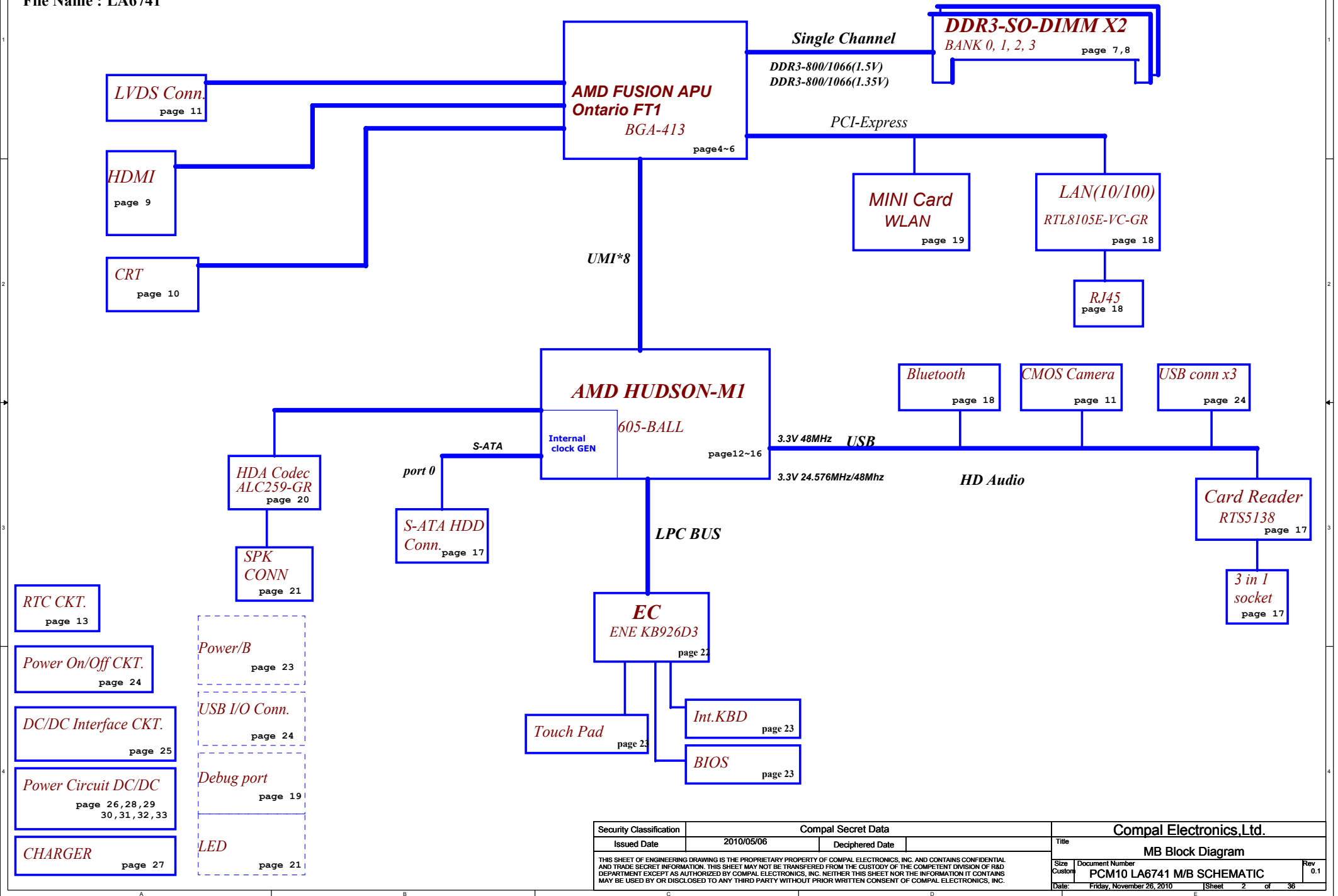
AMD APU Ontario-FT1+ FCH Hudson-M1

2010-11-30

REV:1.0

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				Size Custom	Document Number PCM10 LA6741 M/B SCHEMATIC
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				[Sheet 1 of 36]	

File Name : LA6741



DDR3 Voltage Rails

<div>power plane</div> <div>State</div>	<div>+B</div> <div>+3VL</div> <div>+5VL</div> <div>+RTCVCC</div>	<div>+5VALW</div> <div>+3VALW</div> <div>+1.1VALW</div>	<div>+1.5V</div>	<div>+5VS</div> <div>+3VS</div> <div>+1.5VS</div> <div>+CPU_CORE</div> <div>+NB_CORE</div> <div>+1.8VS</div> <div>+0.75VS</div> <div>+1.1VS</div> <div>+1.0VS</div>
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

@	Reserve
CONN@	ME CONNECTOR
8105E@	100M LAN function
8111E@	GLAN function
REAL@	ALC259-GR
VIA@	V1802T
ROM@	not support flash ROM
FROM@	Support flash ROM

FCH SM Bus0 address

Device	HEX	Address	Device	HEX	Address
SDDIM I	A0	1010 0000	WLAN		
SDDIM II	A2	1010 0010			

FCH SM Bus1 address

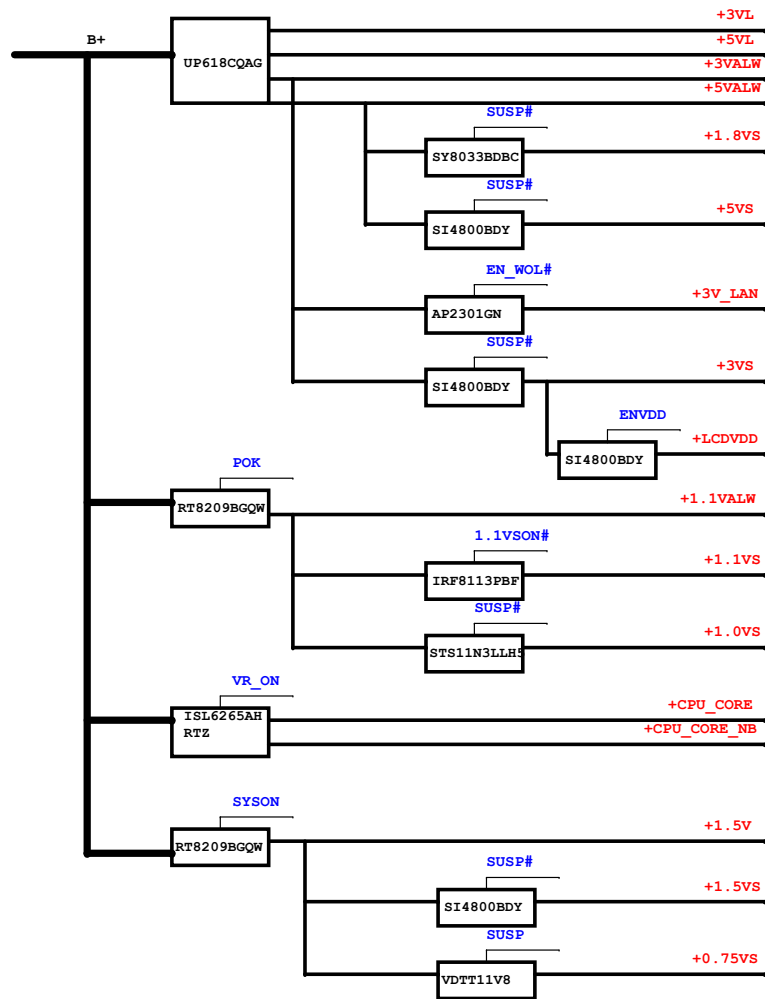
EC SM Bus1 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X b	APU internal thermal sensor		1001 100X b

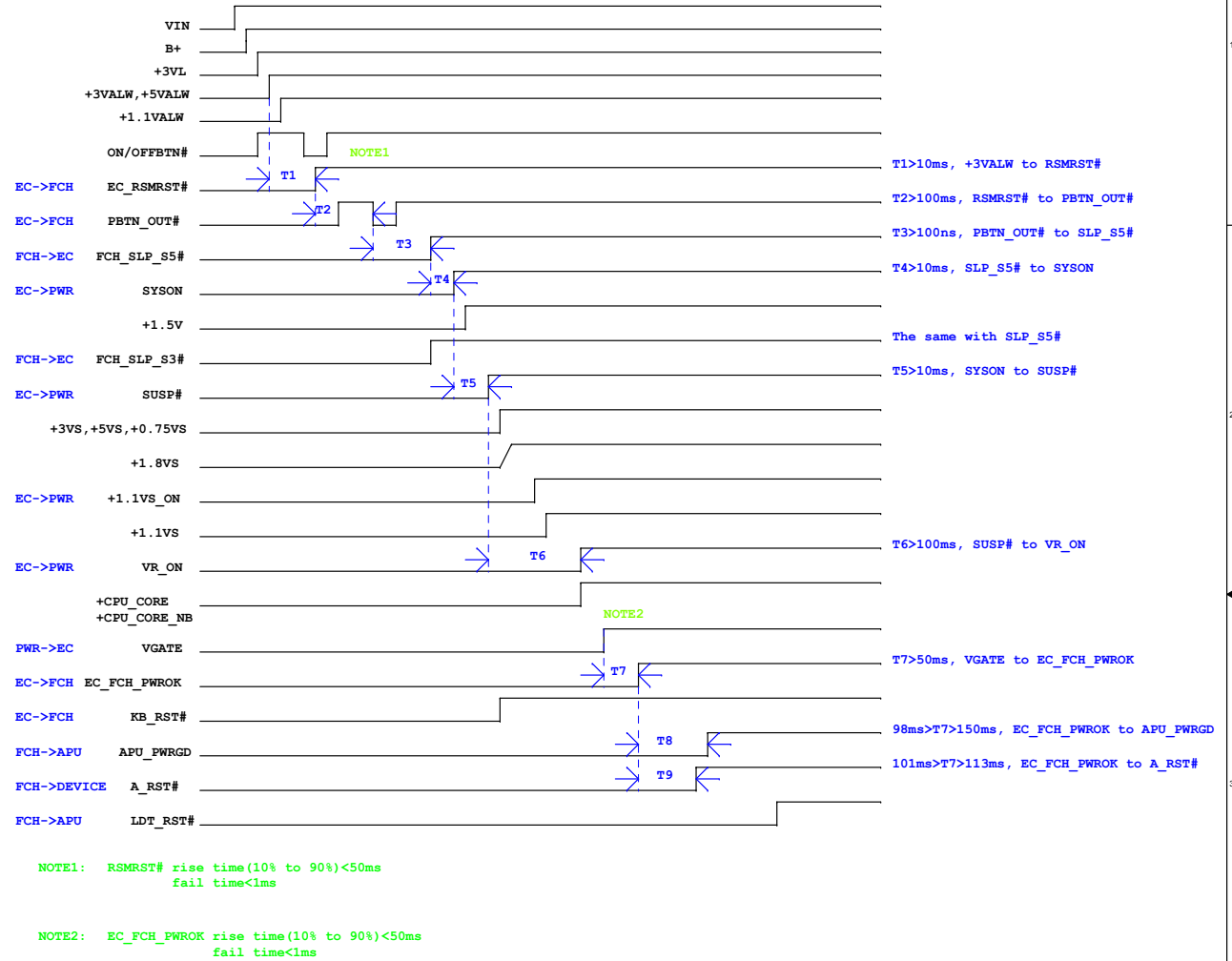
EC SM Bus2 address

	SOURCE	POWER PLAN	HDMI	LVDS	CRT	FCH	CPU CORE	SDDIM I/II	WLAN	BATT	APU
TDP1_AUXP TDP1_AUXN	APU	+3VS	V								
LTDP0_AUXP LTDP1_AUXN	APU	+3VS		V +5VS							
DAC_SCL DAC_SDA	APU	+3VS			V +5VS						
SIC SID	APU	+3VS				V +3VALW					
SVC SVD	APU	+1.8VS					V				
SMB_FCH_CK0 SMB_FCH_DA0	FCH	+3VS						V			
SMB_FCH_CK1 SMB_FCH_DA1	FCH	+3VALW							V		
SMB_EC_CK1 SMB_EC_DA1	EC	+5VALW								V	
SMB_EC_CK2 SMB_EC_DA2	EC	+3VS									V

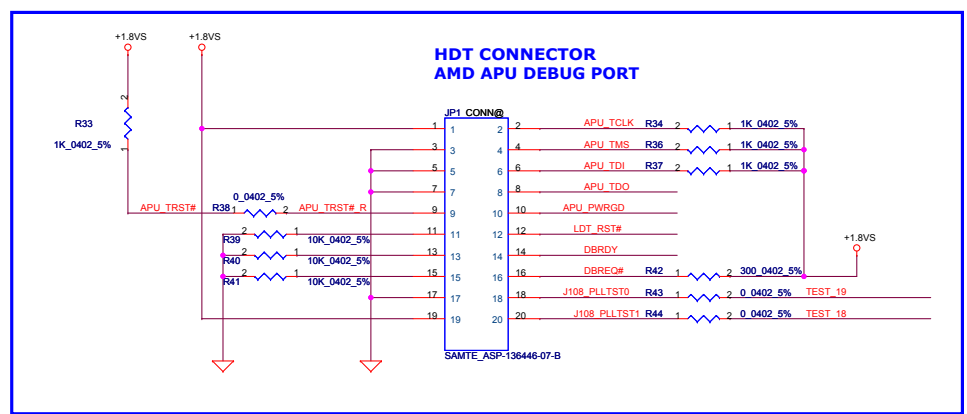
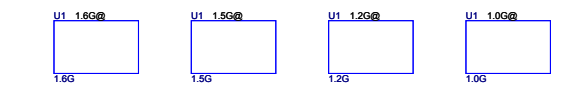
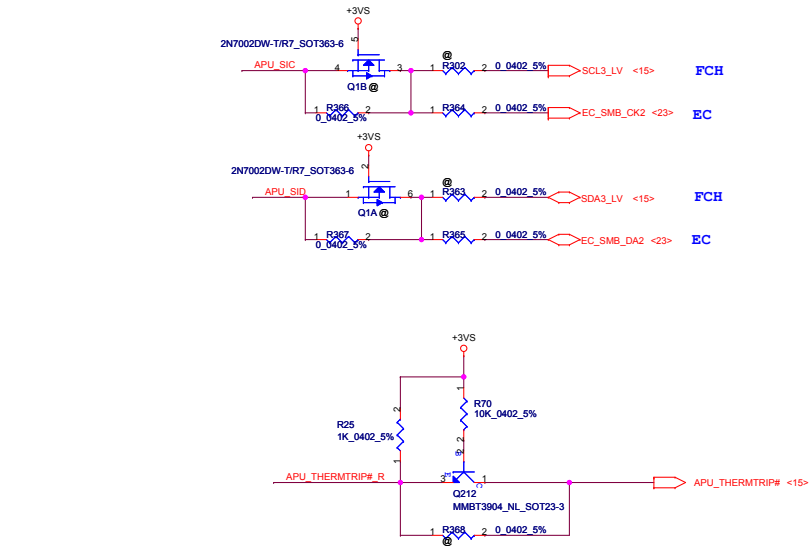
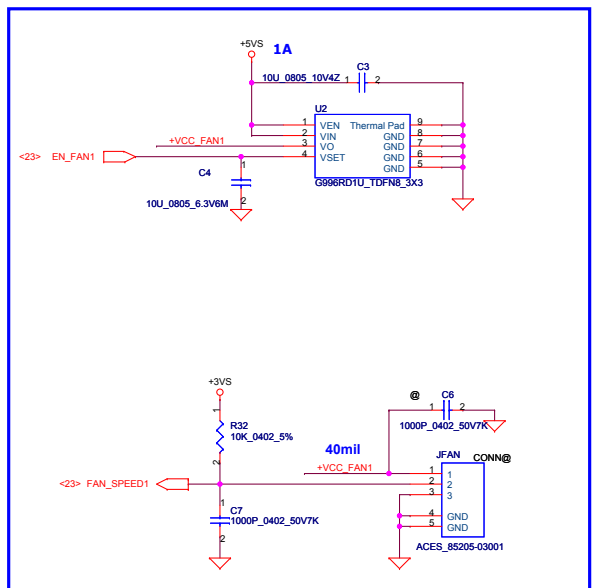
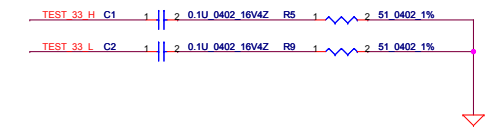
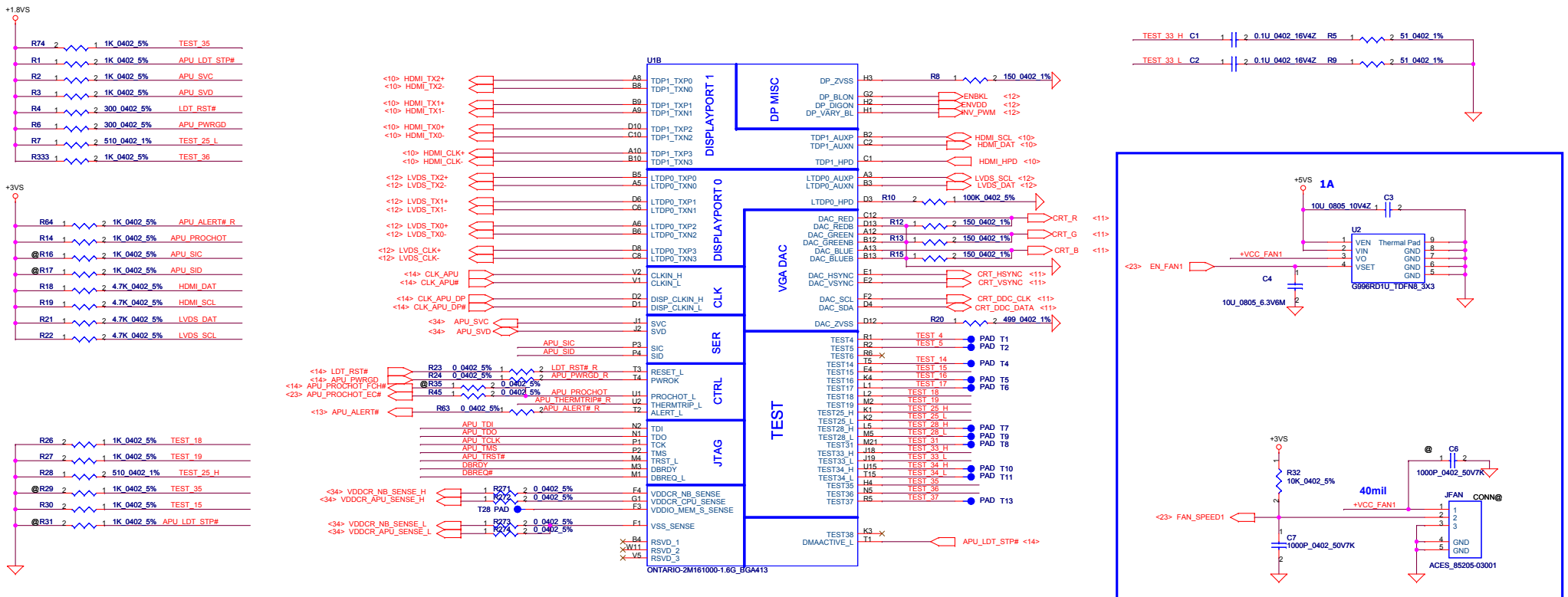
POWER MAP

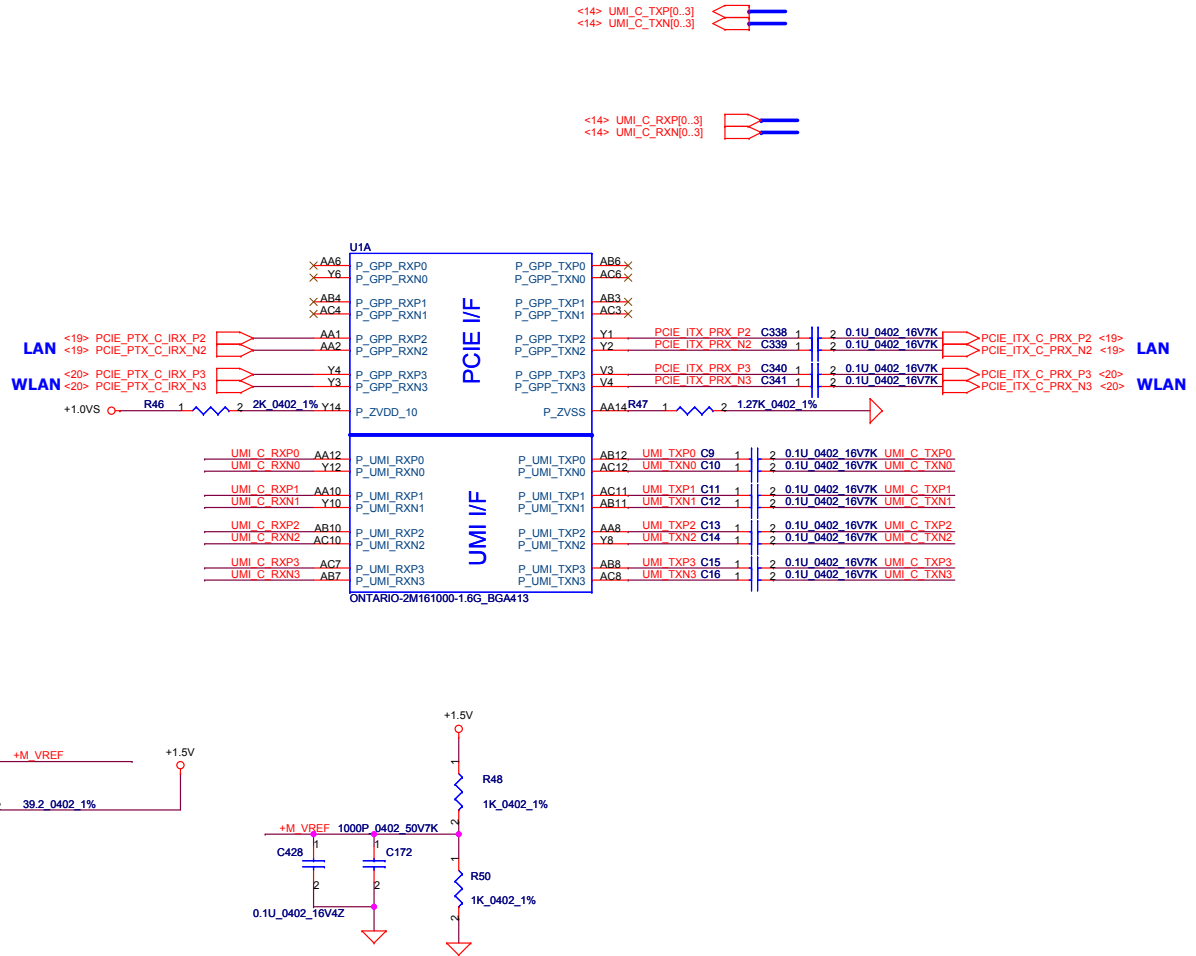
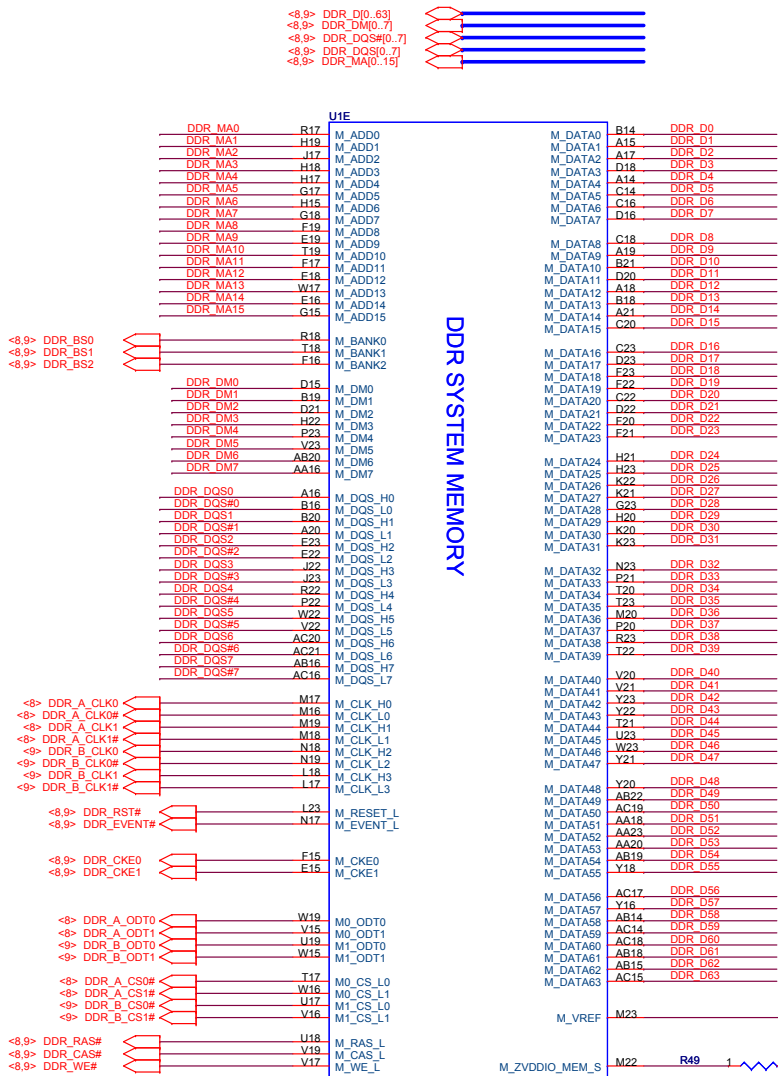


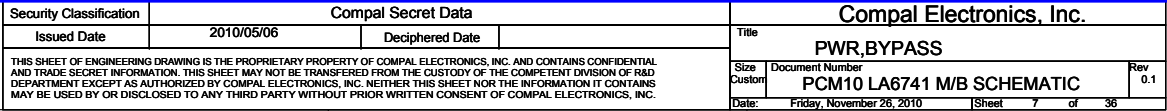
POWER SEQUENCE

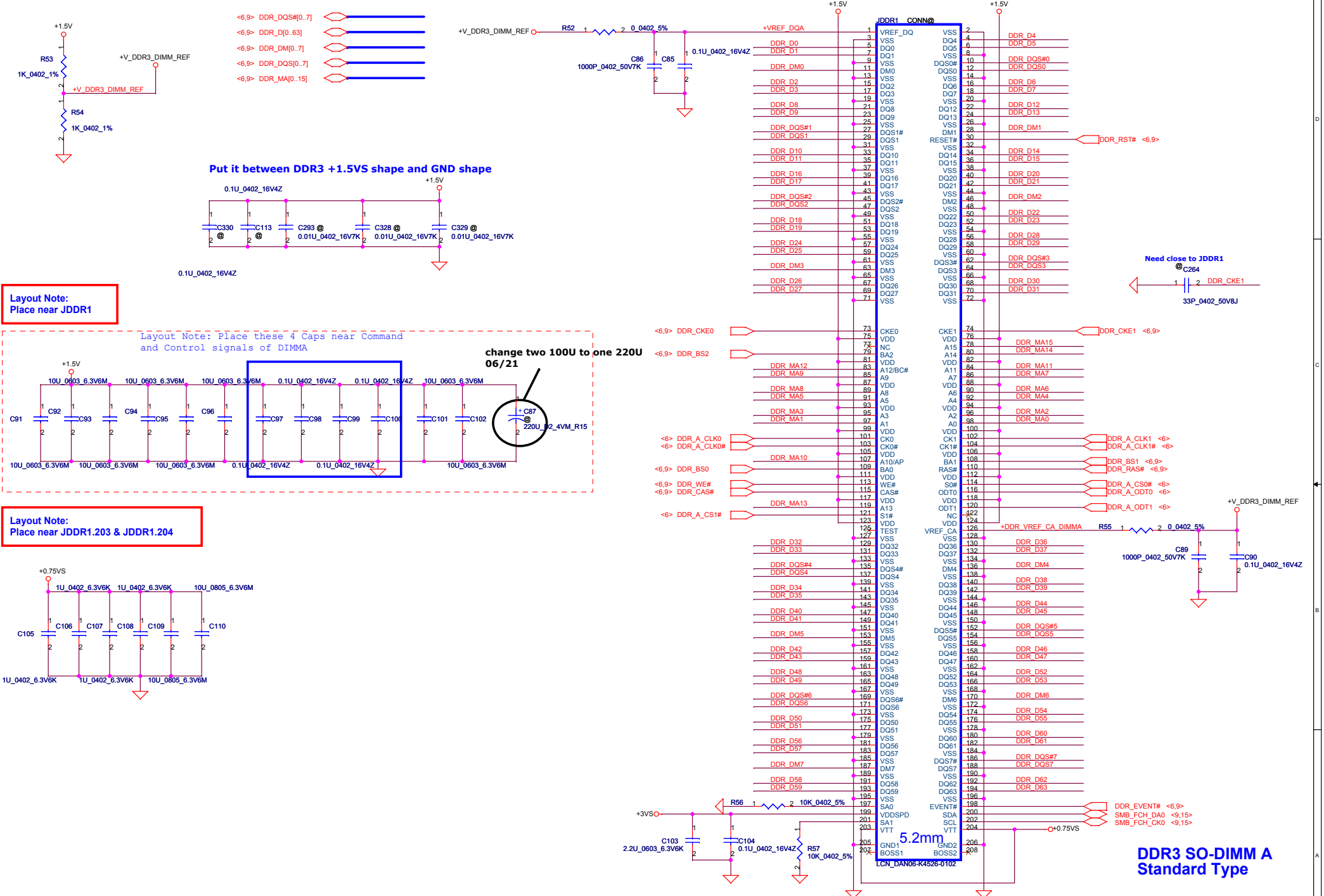


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Size		Document Number		Rev	
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PCMC10 LA6741 M/B SCHEMATIC				0.1	

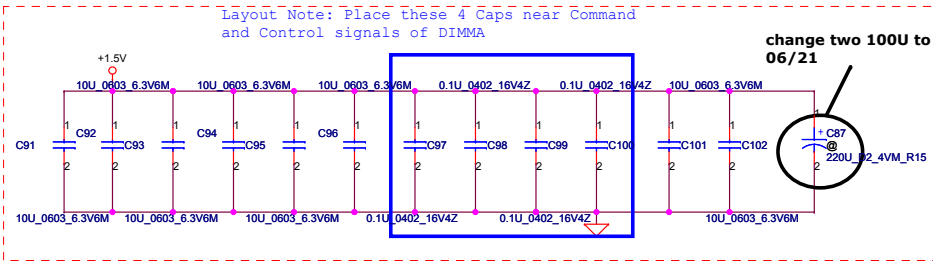




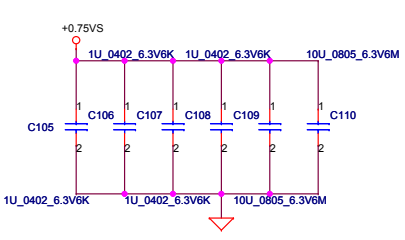




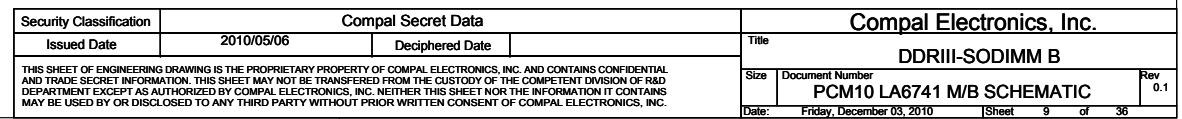
Layout Note:
Place near JDDR1



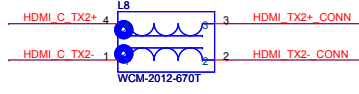
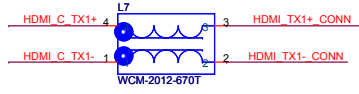
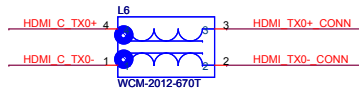
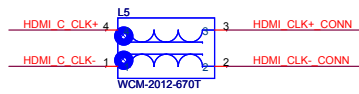
Layout Note:
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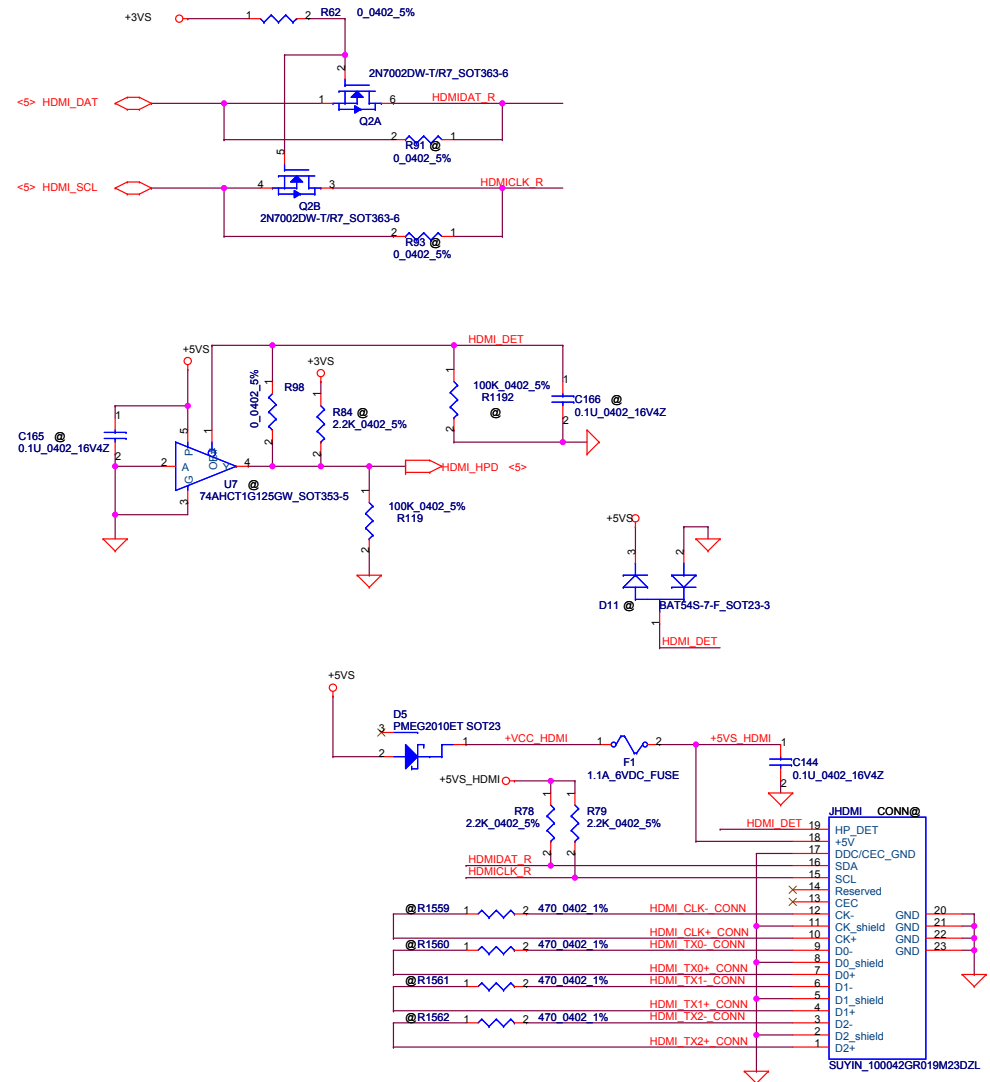
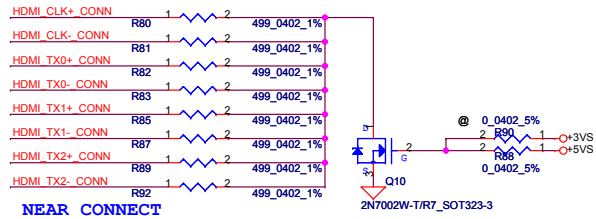
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Issued Date	2010/05/06	Deciphered Date	2010/02/04	DDR3 SO-DIMM A	
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				Date: Friday, December 03, 2010	Rev 0.1



<S> HDMI_CLK-	HDMI_CLK-	C136	1	2	0.1U_0402_16V7K	HDMI_C_CLK-
<S> HDMI_CLK+	HDMI_CLK+	C137	1	2	0.1U_0402_16V7K	HDMI_C_CLK+
<S> HDMI_TX2+	HDMI_TX2+	C138	1	2	0.1U_0402_16V7K	HDMI_C_TX2+
<S> HDMI_TX2-	HDMI_TX2-	C139	1	2	0.1U_0402_16V7K	HDMI_C_TX2-
<S> HDMI_TX1+	HDMI_TX1+	C140	1	2	0.1U_0402_16V7K	HDMI_C_TX1+
<S> HDMI_TX1-	HDMI_TX1-	C141	1	2	0.1U_0402_16V7K	HDMI_C_TX1-
<S> HDMI_TX0+	HDMI_TX0+	C142	1	2	0.1U_0402_16V7K	HDMI_C_TX0+
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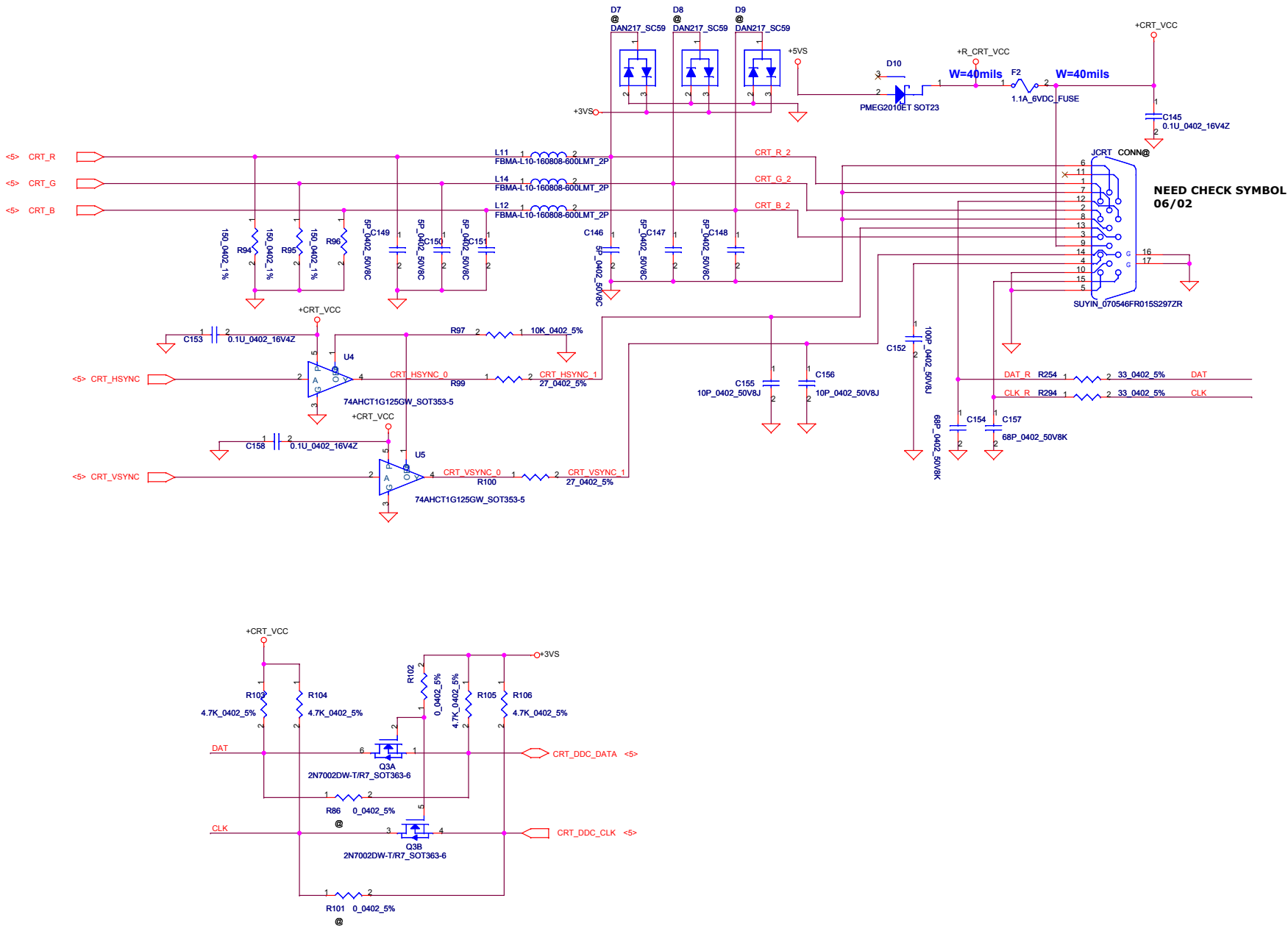


HDMI_C_CLK+	@	R65	1	2	0.0402_5%	HDMI_CLK+ CONN
HDMI_C_CLK-	@	R66	1	2	0.0402_5%	HDMI_CLK- CONN
HDMI_C_TX0+	@	R67	1	2	0.0402_5%	HDMI_TX0+ CONN
HDMI_C_TX0-	@	R68	1	2	0.0402_5%	HDMI_TX0- CONN
HDMI_C_TX1+	@	R71	1	2	0.0402_5%	HDMI_TX1+ CONN
HDMI_C_TX1-	@	R72	1	2	0.0402_5%	HDMI_TX1- CONN
HDMI_C_TX2+	@	R73	1	2	0.0402_5%	HDMI_TX2+ CONN
HDMI_C_TX2-	@	R75	1	2	0.0402_5%	HDMI_TX2- CONN



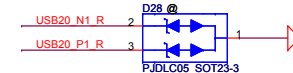
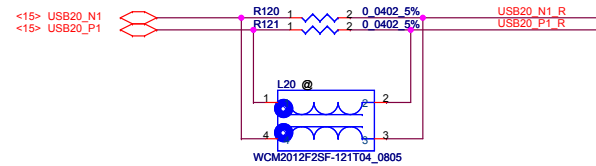
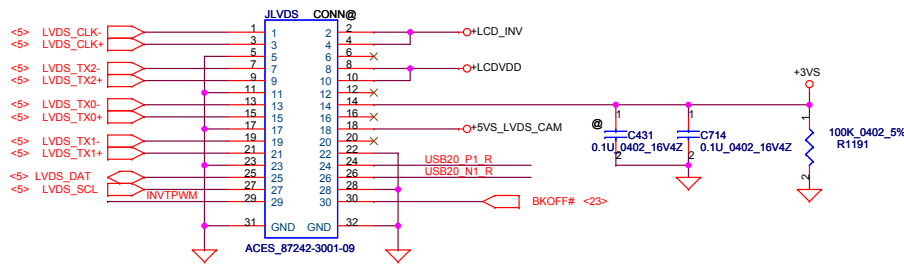
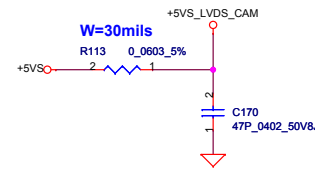
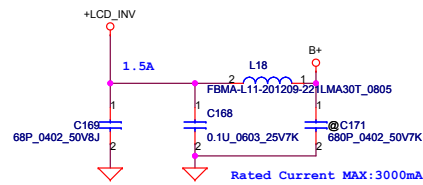
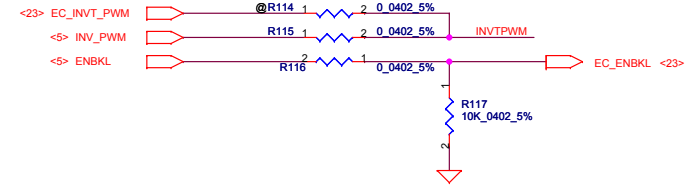
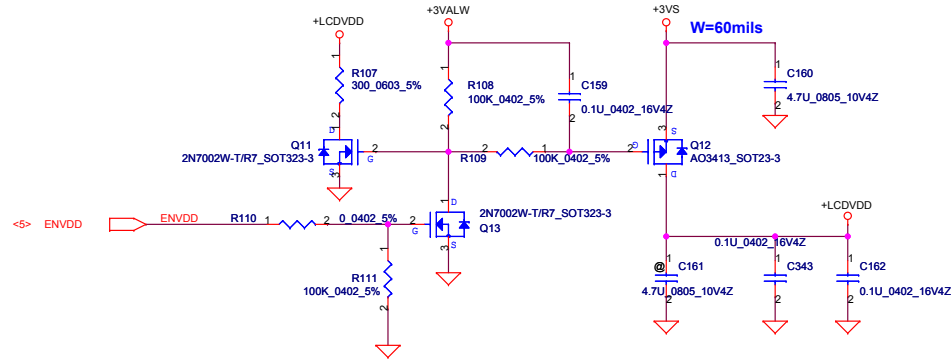
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CRT Connector



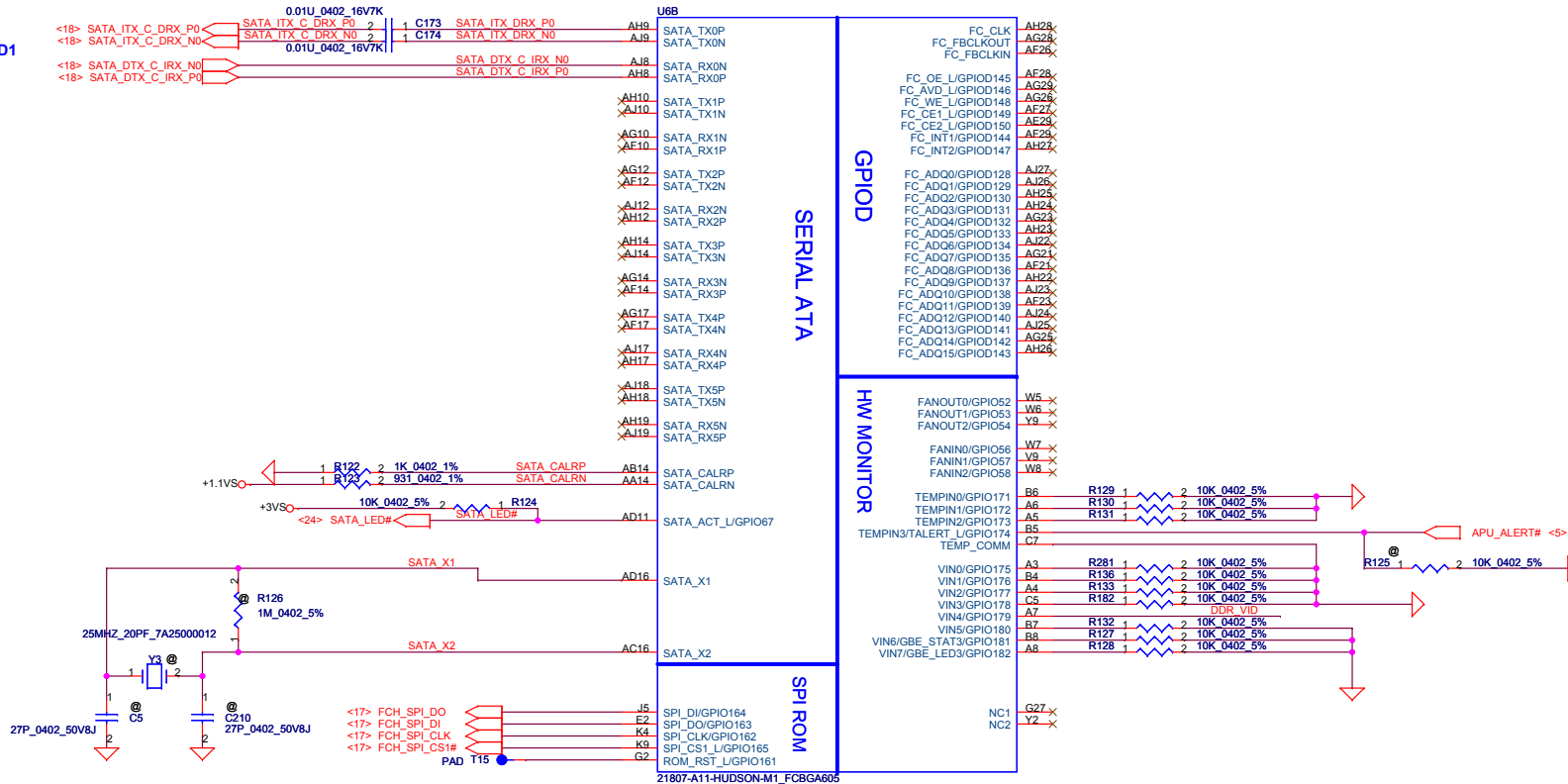
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LCD POWER CIRCUIT

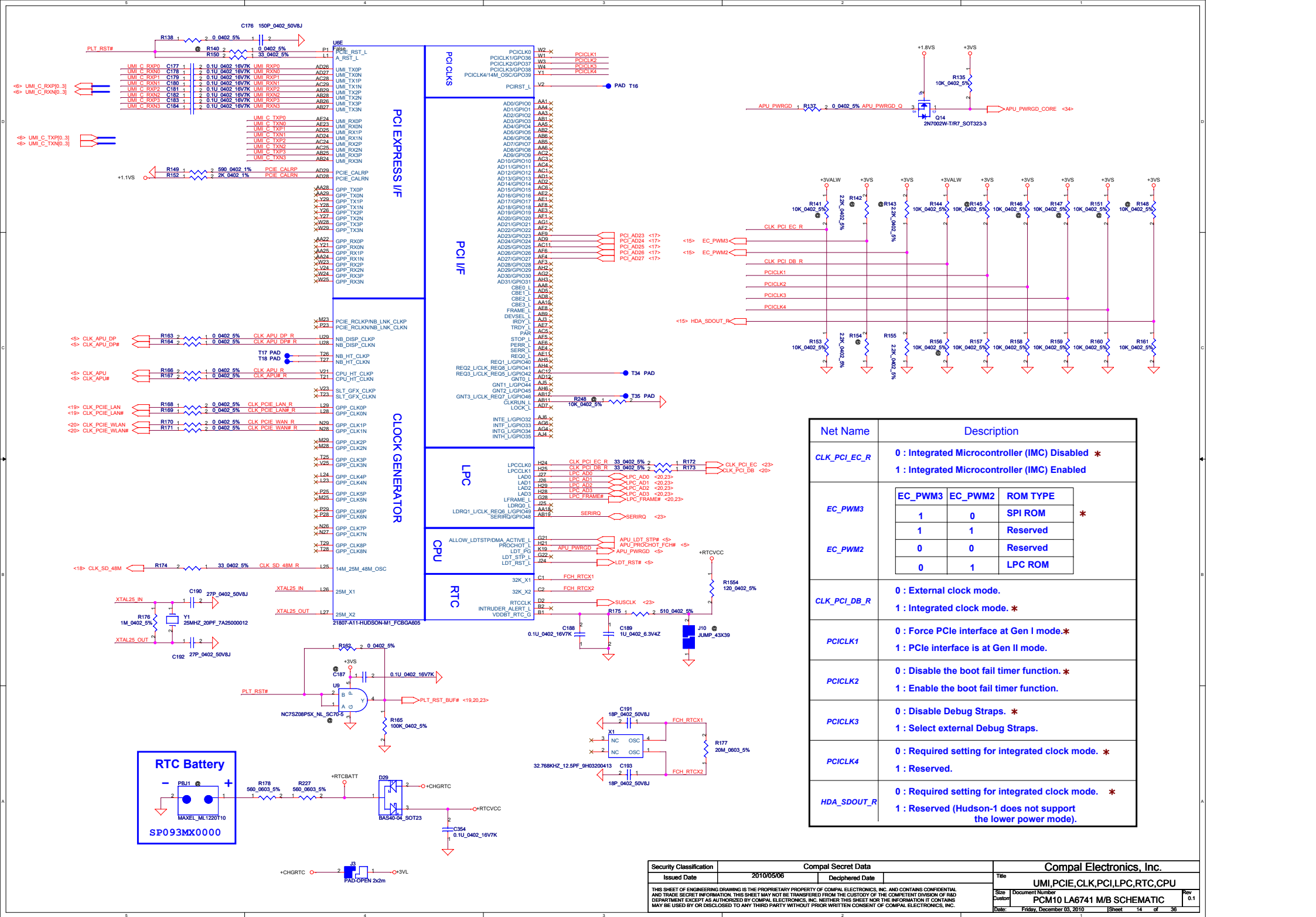


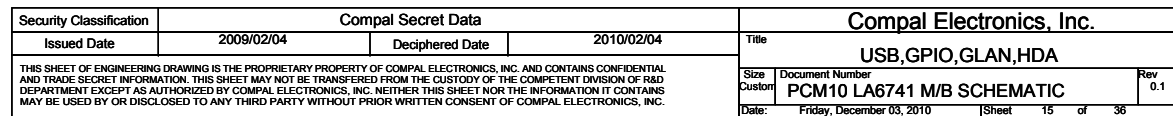
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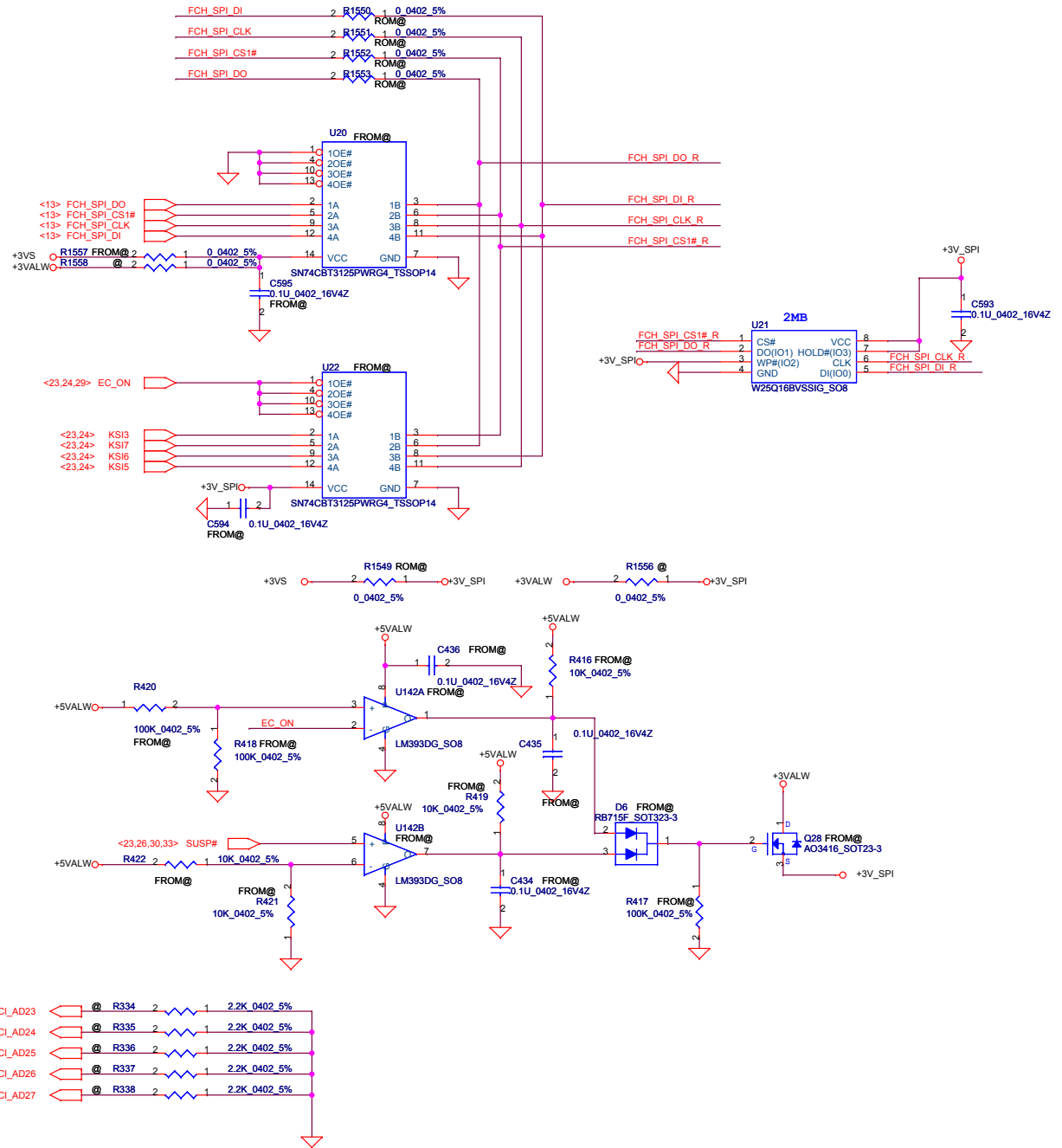
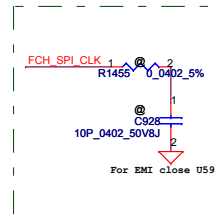
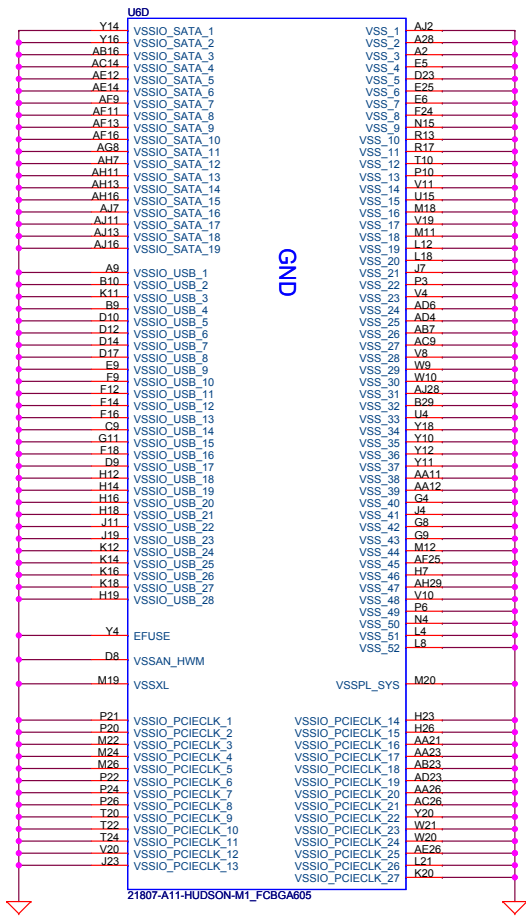
SATA for HDD1



DDR_VID	DDR voltage
0	+1.5V
1	+1.35V



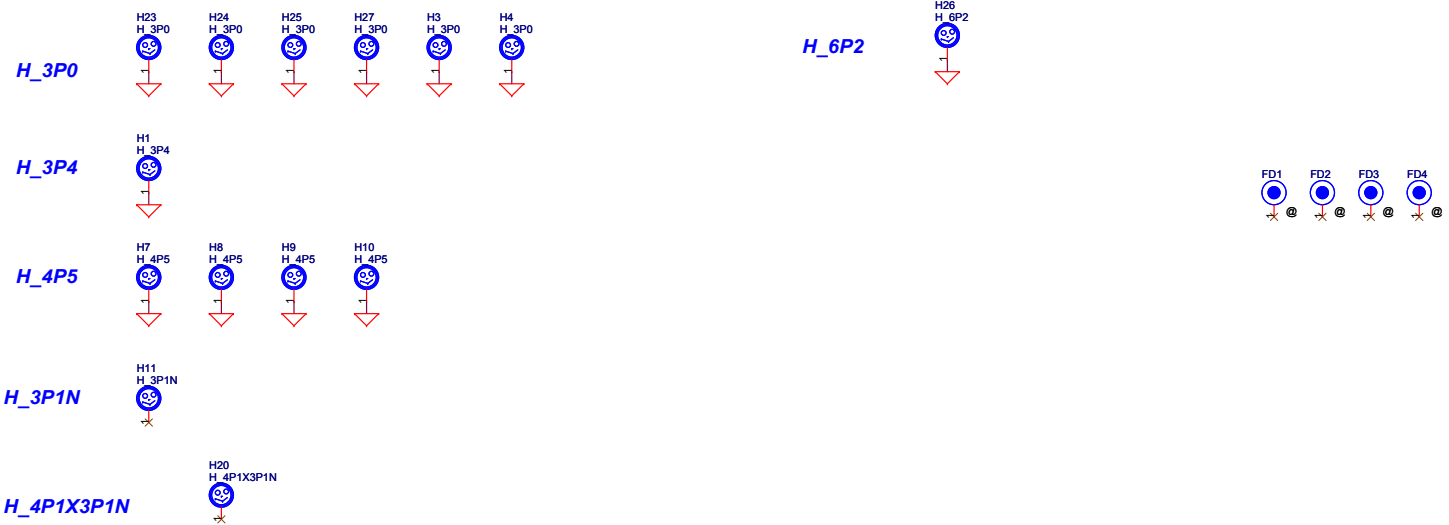
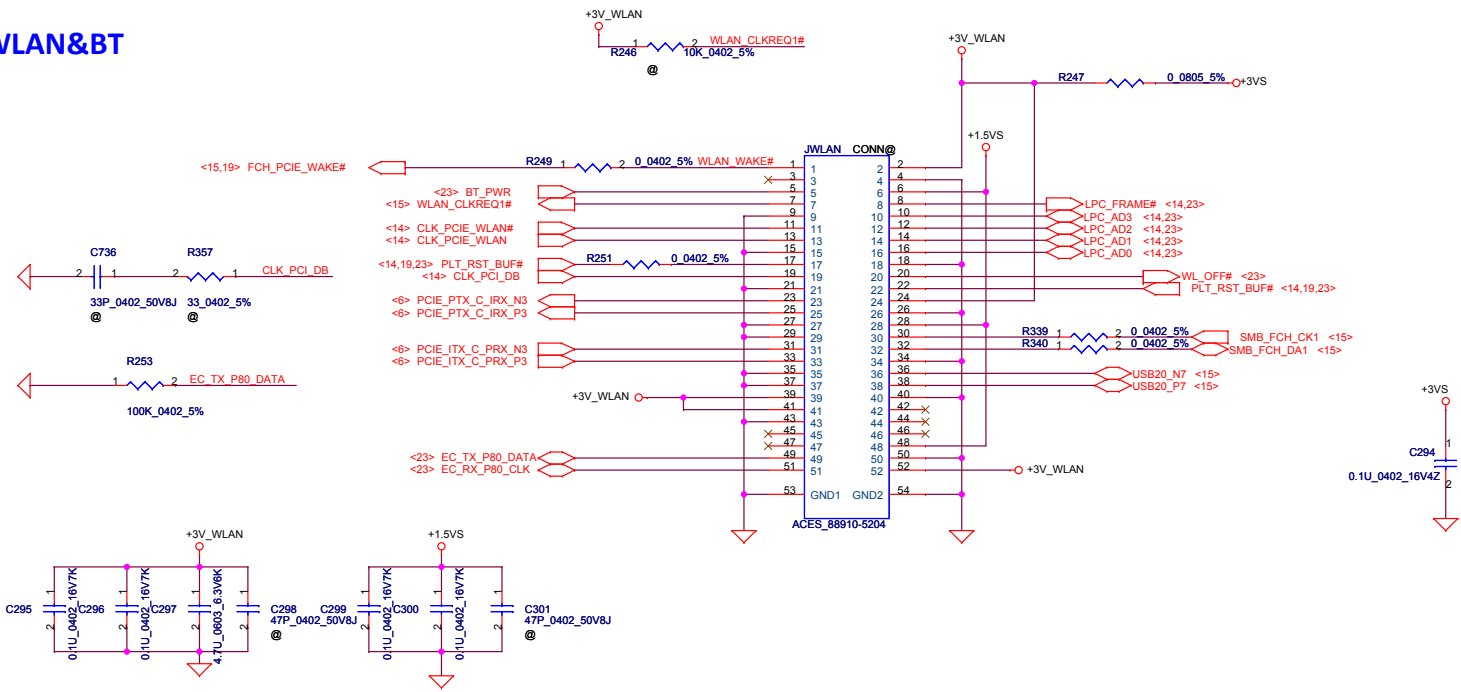




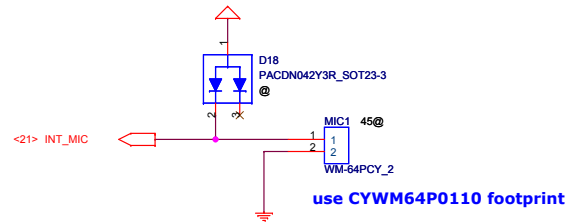
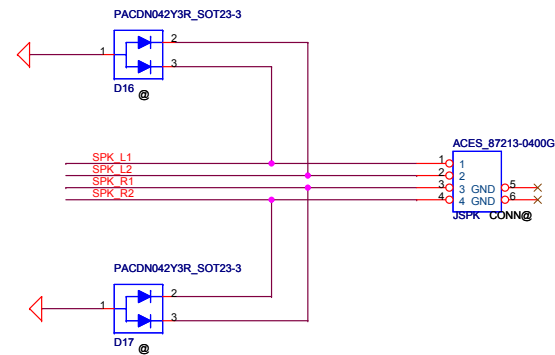
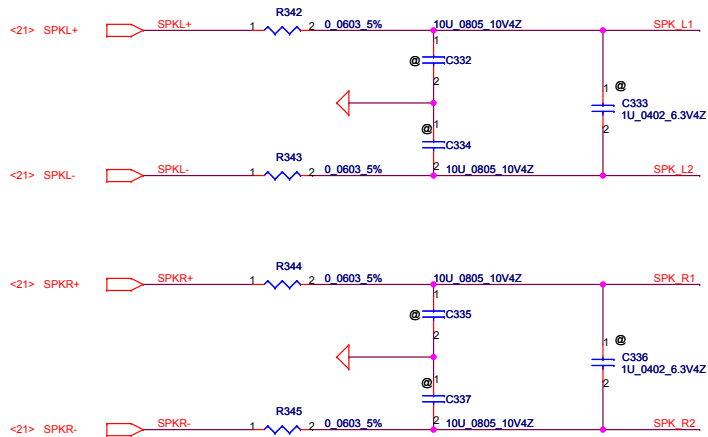
Net Name	Description
PCI_AD27	0 : Bypass internal PLL clock 1 : Use internal PLL-generated PLL CLK *
PCI_AD26	0 : ILA auto run enable 1 : ILA auto run disable *
PCI_AD25	0 : Bypass internal FC Clk 1 : Use internal PLL FC Clk * NEED CHECK
PCI_AD24	0 : Getting the value from I2C EPROM 1 : Disable I2C ROM * NEED CHECK
PCI_AD23	0 : Reserved 1 : Required setting (use ROMTYPE straps to determine the ROM type) *

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GND		
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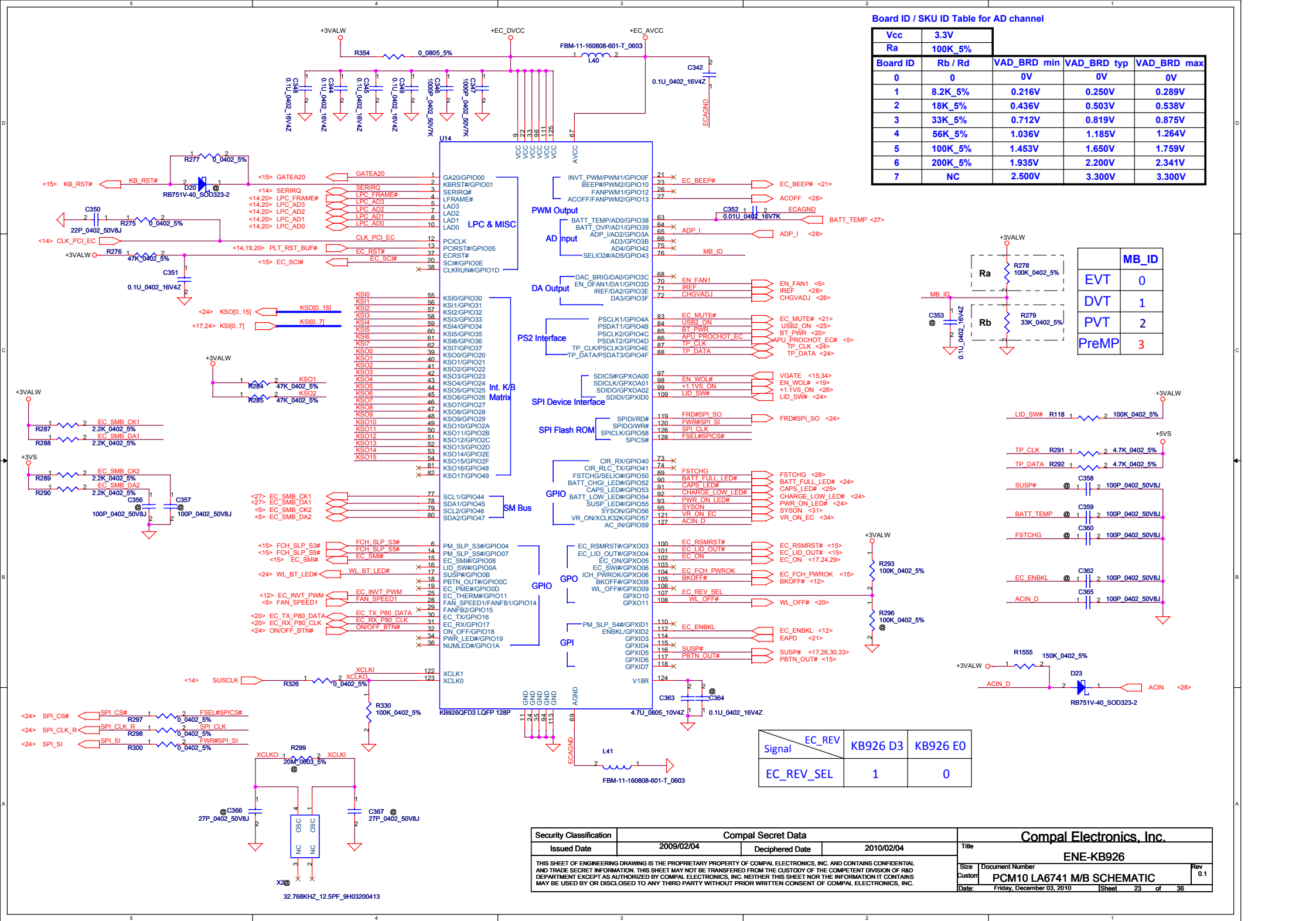
WLAN&BT



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2010/02/04		Title		WLAN&BT&SCREW	
Size		Document Number		Rev	
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Board ID / SKU ID Table for AD channel

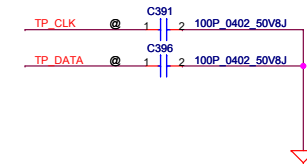
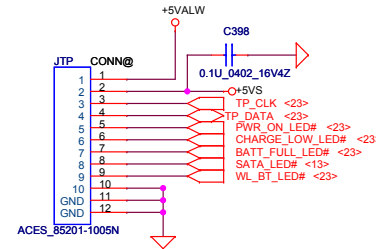
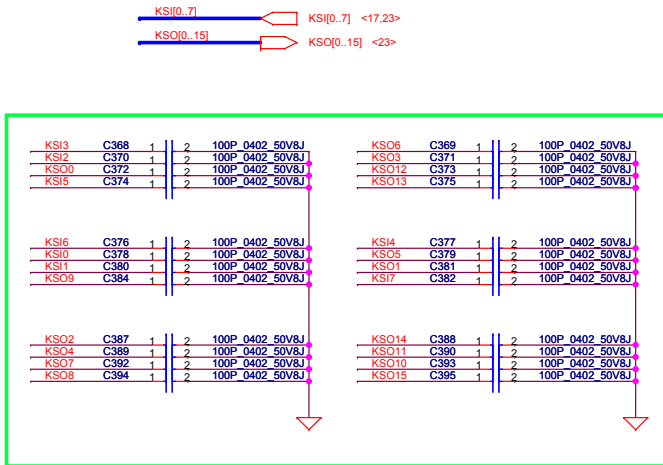
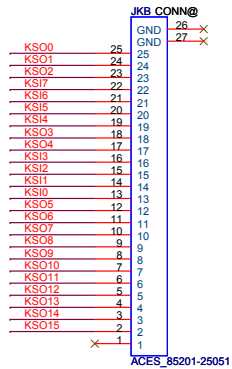
Board ID	3.3V		VAD_BRD min	VAD_BRD typ	VAD_BRD max
	Vcc	Ra			
0	0	100K_5%	0V	0V	0V
1	8.2K_5%		0.216V	0.250V	0.289V
2	18K_5%		0.436V	0.503V	0.538V
3	33K_5%		0.712V	0.819V	0.875V
4	56K_5%		1.036V	1.185V	1.264V
5	100K_5%		1.453V	1.650V	1.759V
6	200K_5%		1.935V	2.200V	2.341V
7	NC		2.500V	3.300V	3.300V

	MB_ID
EVT	0
DVT	1
PVT	2
PreMP	3

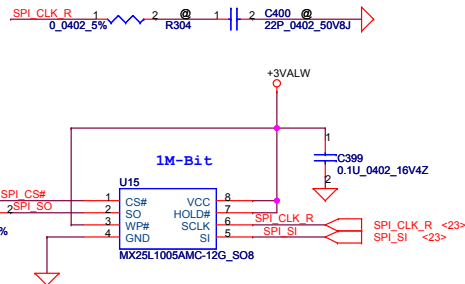
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EC_REV_SEL		1	0

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Size	Document Number	Rev		Date	
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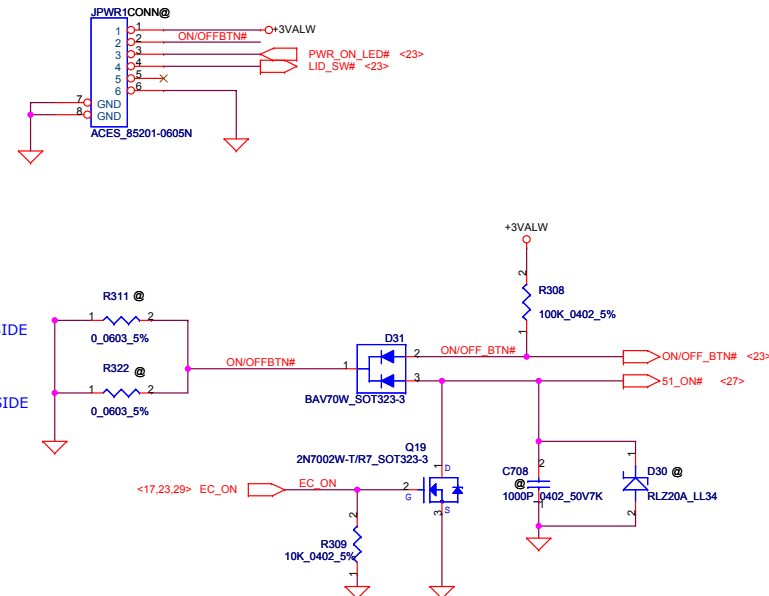
INT_KBD Conn.



EC ROM

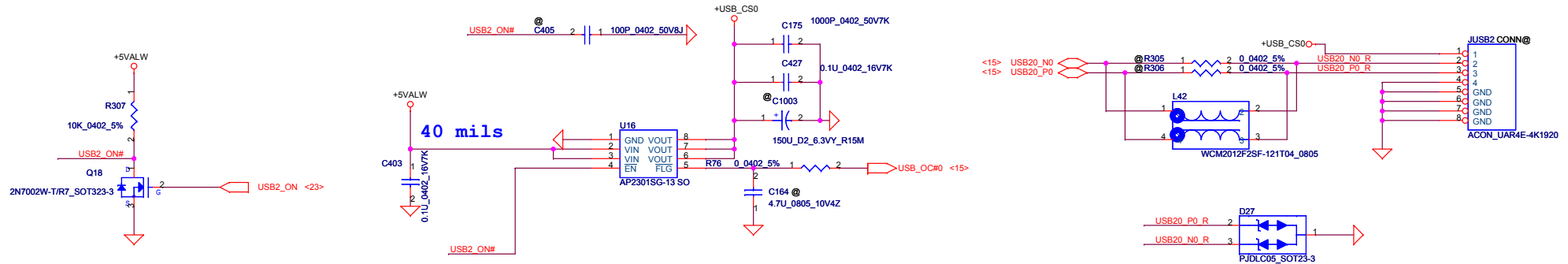


Power BTN Board Conn

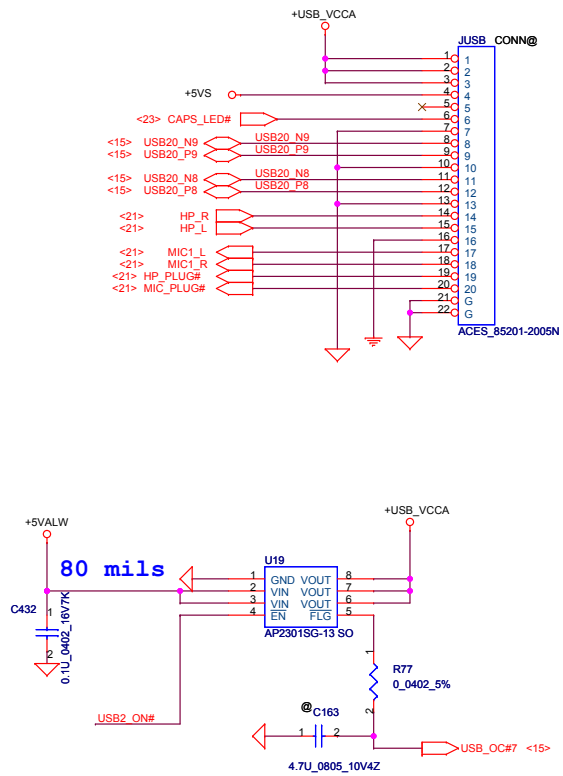


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Date: Friday, December 03, 2010				Rev 0.1
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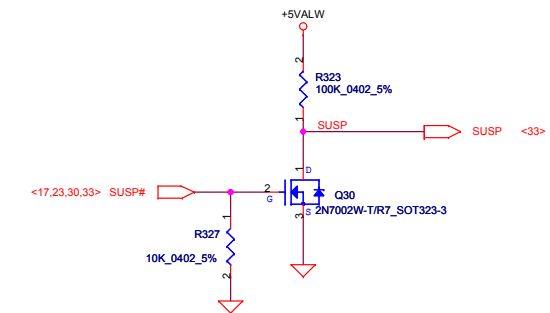
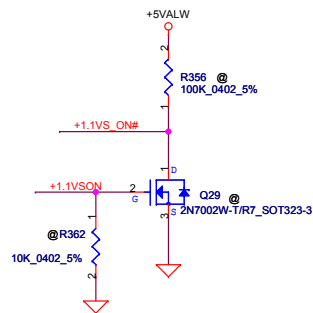
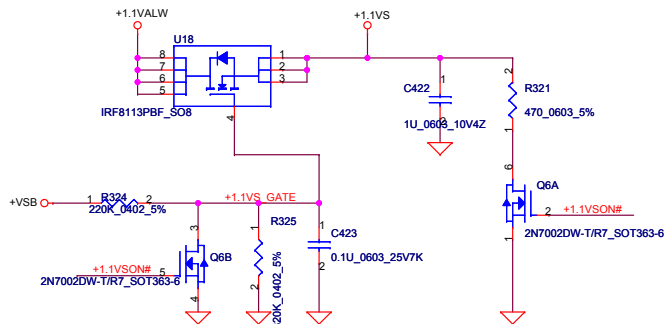
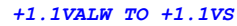
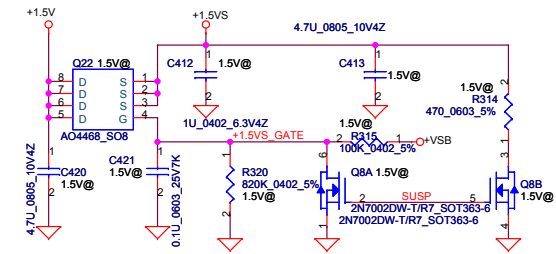
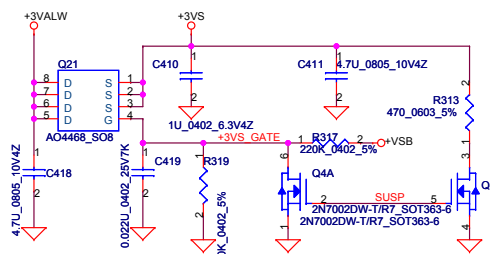
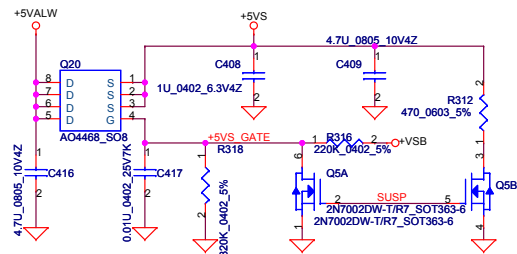
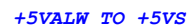
USB PORT0



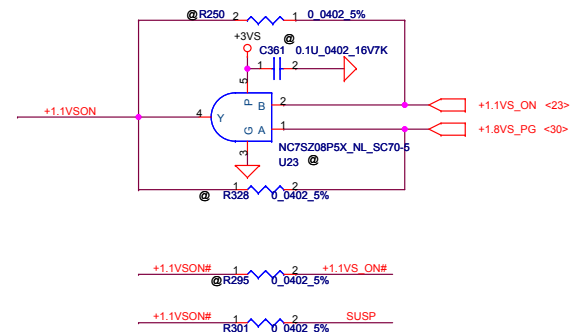
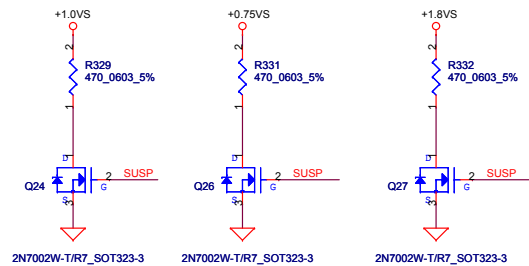
USB Conn



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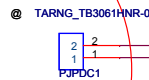


DISCHARGE

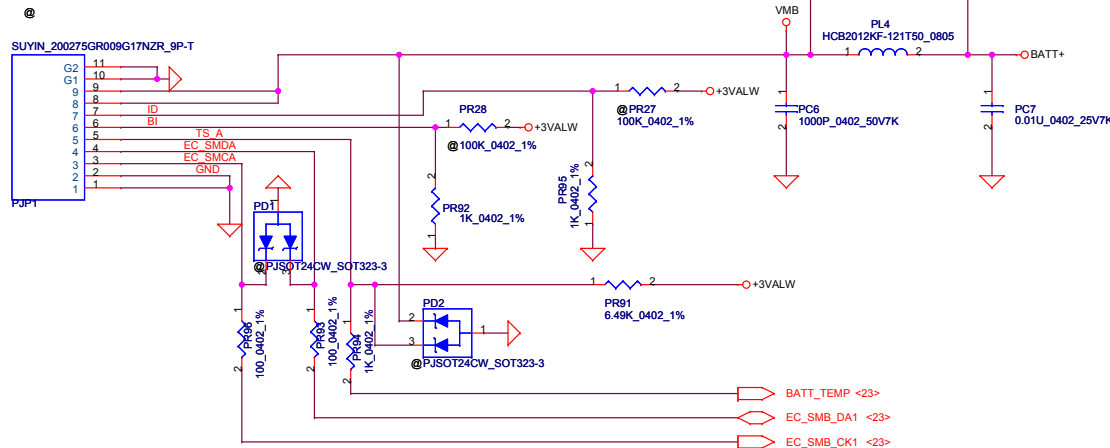


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				Size	Document Number	Rev
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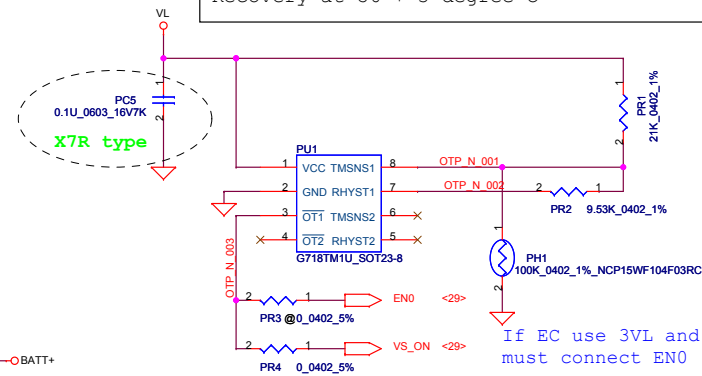
P/N:DC30100CB00



need confirm: ME give us battery connector P/N is DC040006H00



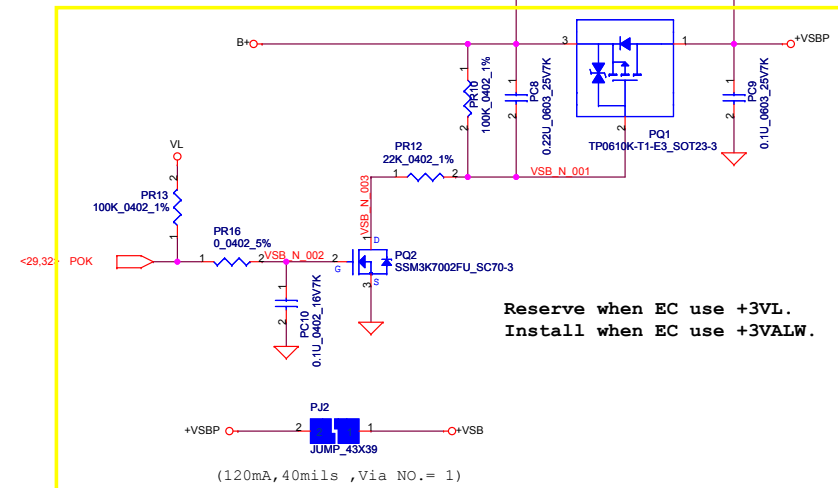
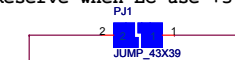
PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



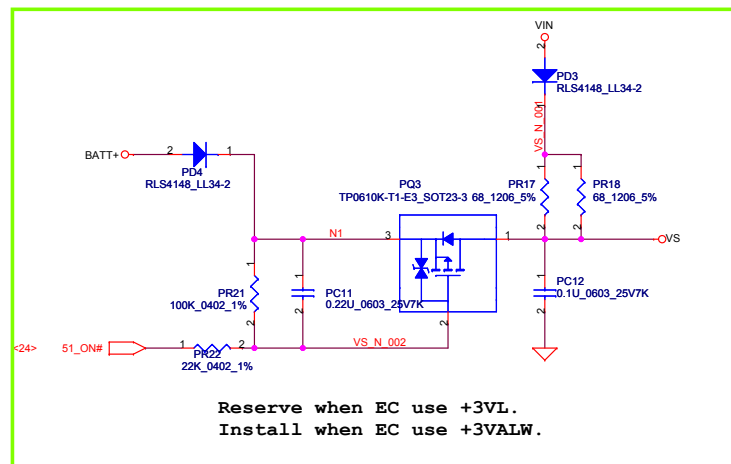
If EC use 3VL and can not detect VGATE, must connect EN0

Install when EC use +3VL
and SUSP was Pull high to +3VL.

Reserve when EC use +3VALW.

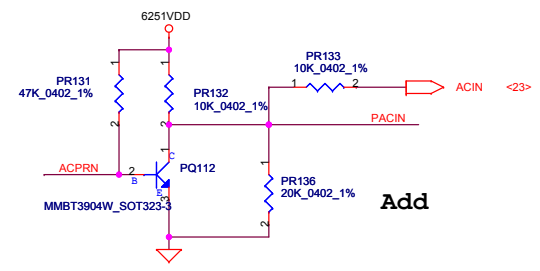


Reserve when EC use +3VL.
Install when EC use +3VALW.

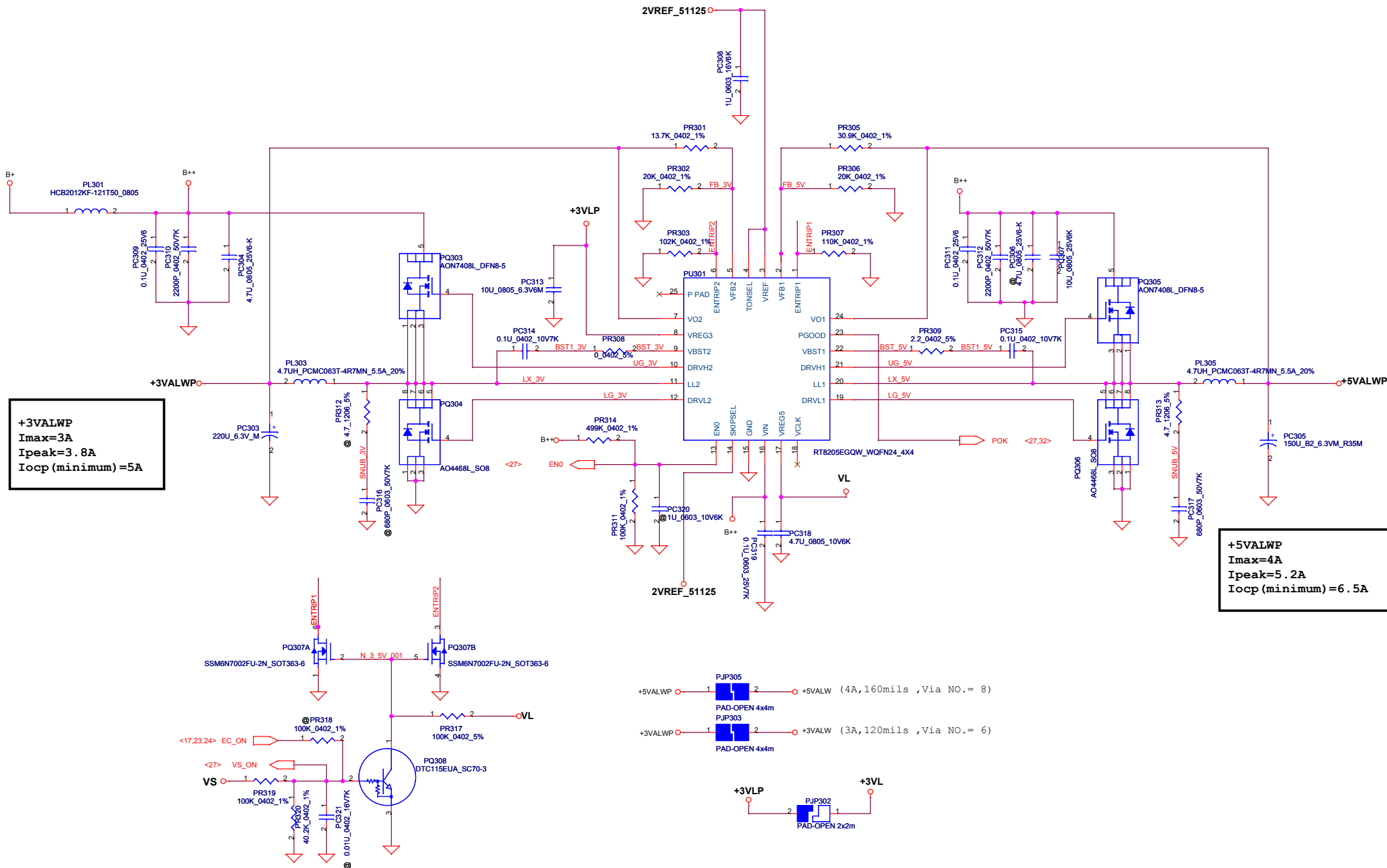


Reserve when EC use +3VL.
Install when EC use +3VALW.

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Size		Document Number		Rev	
		PCM10 LA6741 M/B SCHEMATIC		0.1	
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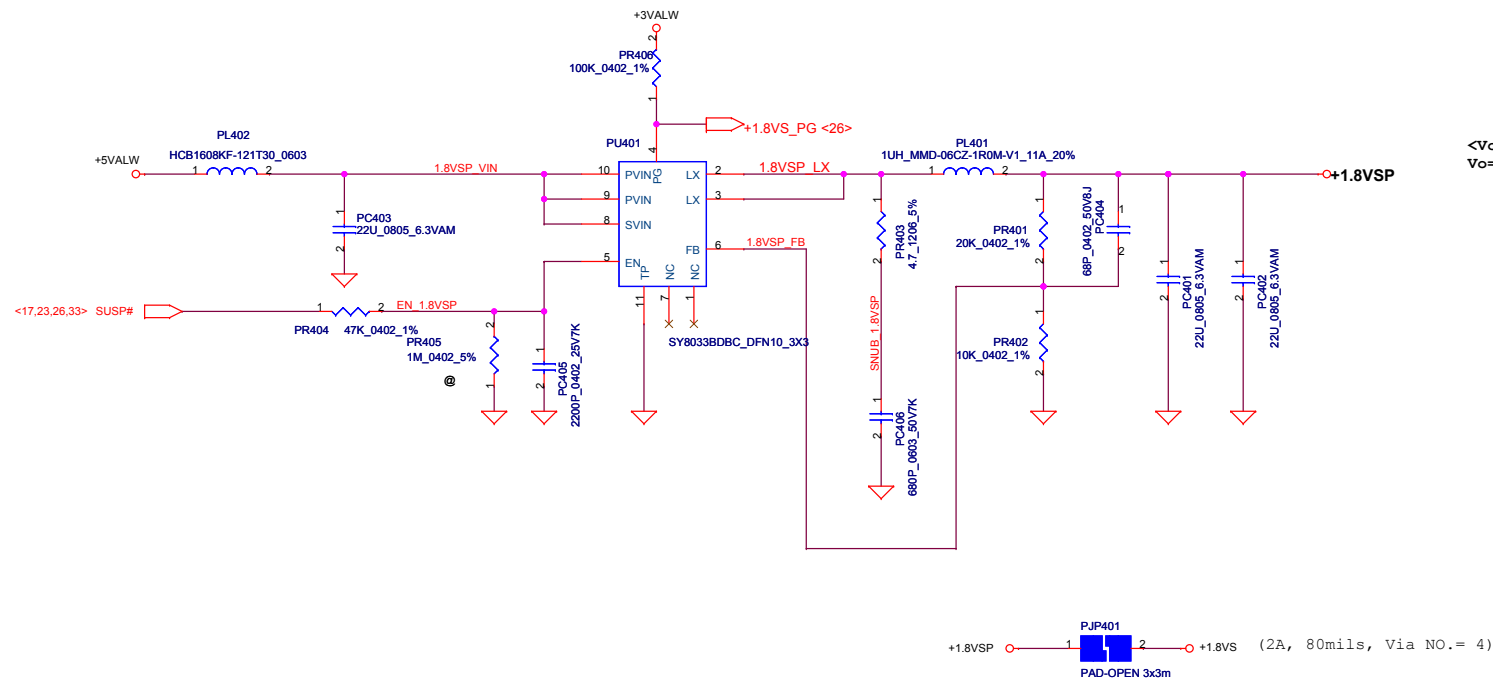


Compal Electronics, Inc.			
CHARGER			
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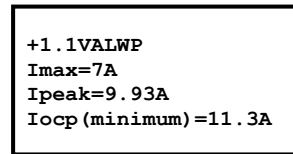


EC:+3VL, reserve PR319, install PR318, PR320 100K
EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

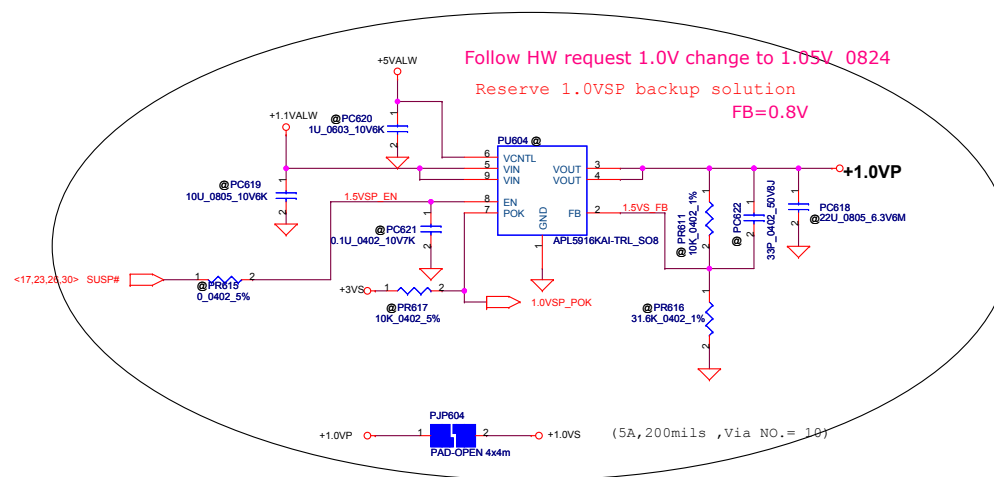
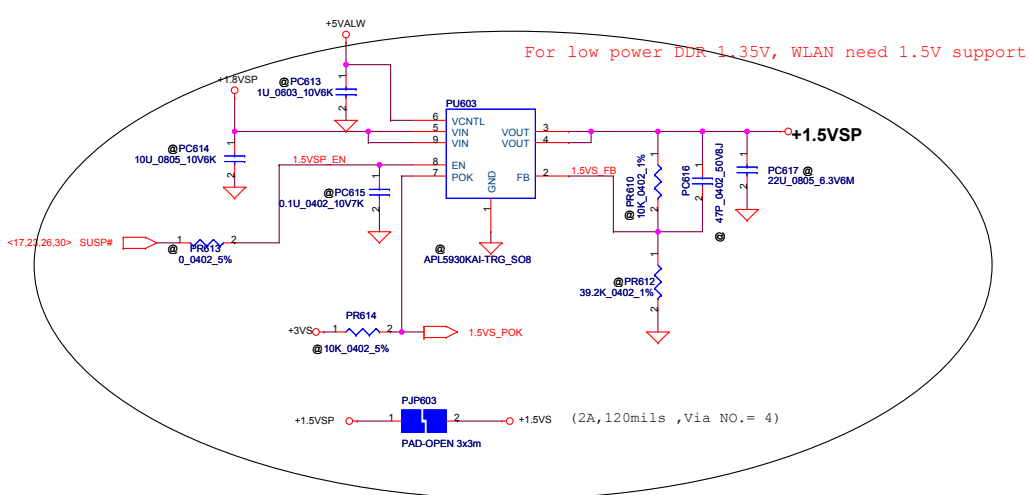
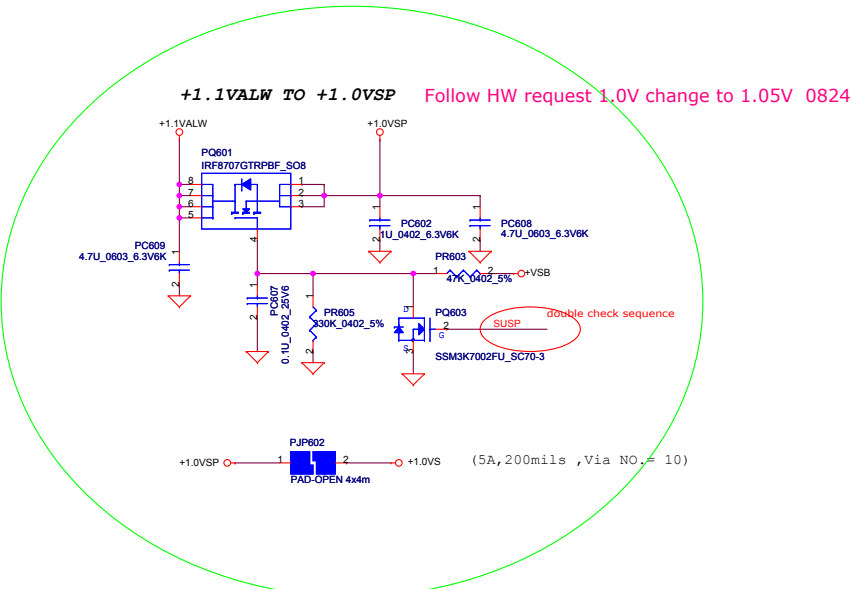
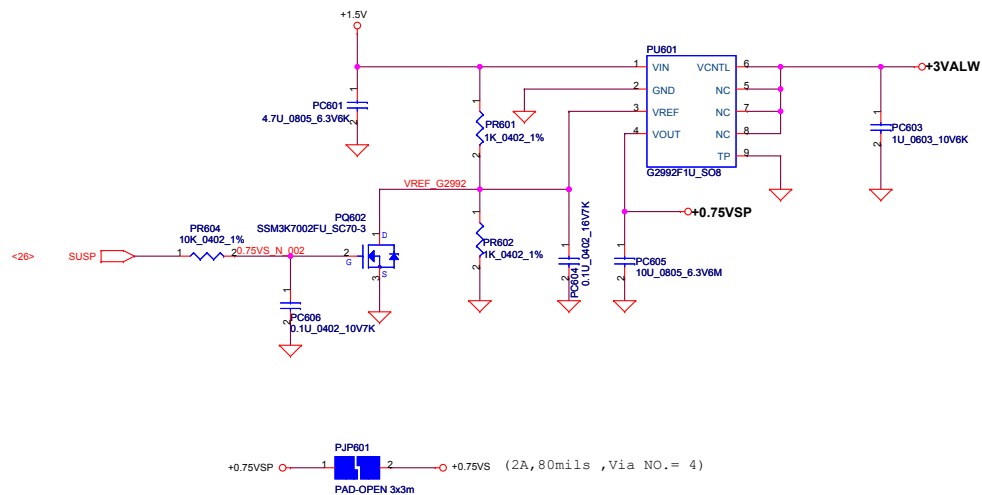
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	3.3VALWP/5VALWP	
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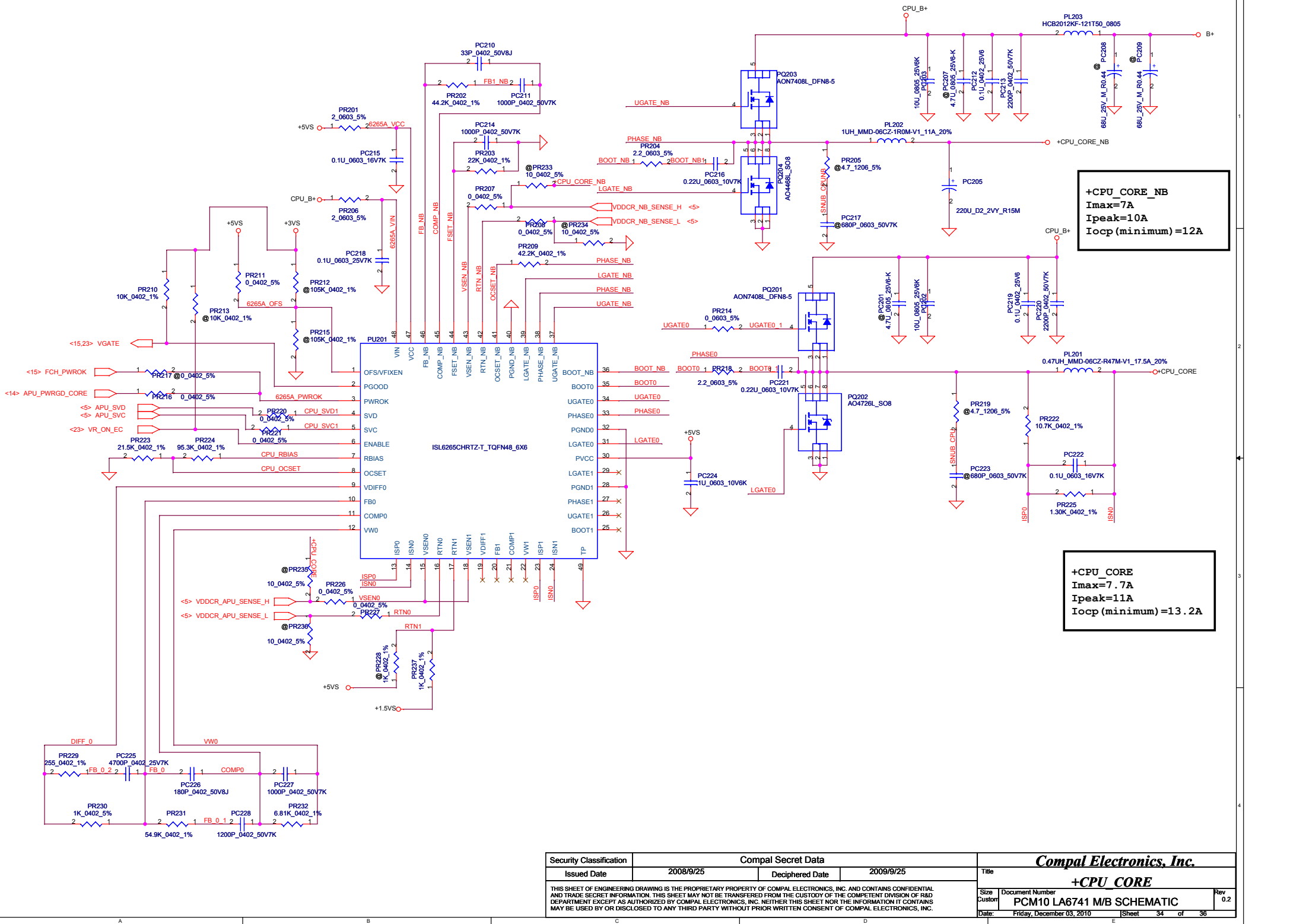
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+CPU_CORE_NB
Imax=7A
Ipeak=10A
Iocp (minimum)=12A

+CPU_CORE
Imax=7.7A
Ipeak=11A
Iocp (minimum)=13.2A

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								Size	Document Number	Rev
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Reason for change	Description	phase	modify	Rev.
1	34	change CPU_CORE input CAP to 68U for height issue.	change CPU_CORE input CAP.	DVT	delete: PC208/PC209 SF000000I80 add: PC208/PC209 SF000000Y00	
2	29	Change 3/5V IC to TPS51125 for business issue.	Change 3/5V IC to TPS51125	DVT	Change 3/5V IC from UP6182 change to TPS51125	
3	29	for common design	3/5V PIN25 can't contact to GND and change PR315 to 100K	DVT	3/5V PIN25 can't contact to GND and change PR315 to 100K	
4	33	Change 0.75V IC to G2992 for business issue.	Change 0.75V IC to G2992	DVT	Change 0.75V IC from UP7711 change to G2992	
5	33	Change PC607 to 0.1U for HW sequence issue.	Change PC607 from 0.01U change to 0.1U	DVT	from SE075103K80 change to SE00000G880	
6	33	Change PR604 and PC606 for HW sequence issue.	Change PR604 from 0 to 10K, and PC606 change to 0.1U for RC delay.	DVT	Change PR604 from 0ohm to 10K, and PC606 from @ change to 0.1U	
7	30	Change PR404 and PC405 for HW sequence issue.	Change PR404 from 0ohm to 47K and PC405 from @ to 2200P	DVT	Change PR404 from 0ohm to 47K and PC405 from @ to 2200P	
8	28	for common design	Delete: PD102, PD103, PD105, PR115, PC111, PC114, PQ109. Add: PR130	DVT	Delete: PD102, PD103, PD105, PR115, PC111, PC114, PQ109. Add: PR130	
9	33	for AMD request 1.0V change to 1.05V	Change PR616 from 39.2K change to 31.6K	DVT	Change PR616 from 39.2K change to 31.6K	
10	27	follow PBL00/01 DC- cable	Change DC-Cable P/N: DC30100CB00	DVT	Change DC-Cable P/N: DC30100CB00	
11	29	Cost down	PC305 change to B2 size	DVT	PC305 P/N from SG020151330 change to SGA00002N80	
12	32	Cost down	change PC701 for cost down.	DVT	PC701 P/N from SGA00004L00 change to SF000002N00	
13	29	Cost down	5V low-side change to AO4468L	DVT	PQ306 P/N from SB00000E310 change to SB000009510	
14	28	CC-CV mode voltage is abnormal	change IC form G5209 change to ISL6251	DVT	PU101 P/N from SA00003TK00 change to SA00001EP80	
15	29	due to change 5V L-side MOS and 3/5V OCP resister,	change 3/5V OCP resister,	DVT	PR303 change to 102K, PR307 change to 65.5K	
16	31	due to change 1.5V L-side MOS and 1.5V OCP resister,	change 1.5V OCP resister,	DVT	PR508 from 15.4K change to 15K	
17	32	due to change 1.1V L-side MOS and 1.1V OCP resister,	change 1.1V OCP resister,	DVT	PR708 from 16.5K change to 15K	
18	34	for cost down change CPU_CORE NB L-side MOS and CORE_NB OCP resister,	change CPU_CORE_NB L-side MOS and CORE_NB OCP resister,	DVT	PL202 from 2.2U change to 1U	
19	34	for cost down change CPU_CORE NB L-side MOS	change CPU_CORE NB L-side MOS	DVT	CPU_CORE_NB L-side MOS from FDS6690 change to AO4468L	
20	34	delete PC208 and PC209 for cost down	delete PC208 and PC209	DVT	delete PC208 and PC209	
21		For DVT phase material short, change P/N	change PC205, PC303, PC501, PC701	PVT	P/N from SF000002N00 change to SF000003I00	
22	33	delete 1.0V LDO for cost down.	delete 1.0V LDO	PVT	delete 1.0V LDO	
24	34	for common design	PIN17 RTN1 net from 5VS change to 1.5V	PVT	PIN17 RTN1 net from 5VS change to 1.5V	
25	29	modify 5V_alw OCP	change PR307 from 65.5K to 86.6K	PVT	P/N change to SD034866280	

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Version Change List (P. I. R. List)for Power Circuit

Item	Page#	Reason for change	Description	phase	modify	Rev.
1	28	Change charge bead to choke for EMI request.	add PL403 (SH00000IY00)	Pre-MP	delete: PL102 add: PL403	
2	28	for common design	Change charge input CAP from 10U to 4.7U	Pre-MP	Change charge input CAP PC104 from 10U to 4.7U	
3	33	PQ601 A04712 maybe cause leakage issue.	Change PQ601 from AO4712 to IRF8707	Pre-MP	Change PQ601 from AO4712 to IRF8707	
4		For DVT phase material short, change P/N	change PC205, PC303, PC501, PC701	Pre-MP	P/N from SF000003I00 change to SF000003000	
5	29	modify 5V_alw OCP	change PR307 from 86.6K to 110K	Pre-MP	P/N change to SD034110380	
6	34	change PC205 to D2 size to meet ME request	change PC205 to D2 size	Pre-MP	change PC205 to D2 size, P/N change to SGA00004L00	
7	34	for common design	PIN17 RTN1 net from 5VS change to 1.5Vs	PVT	PIN17 RTN1 net from 5VS change to 1.5Vs	
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